

FIG. 1

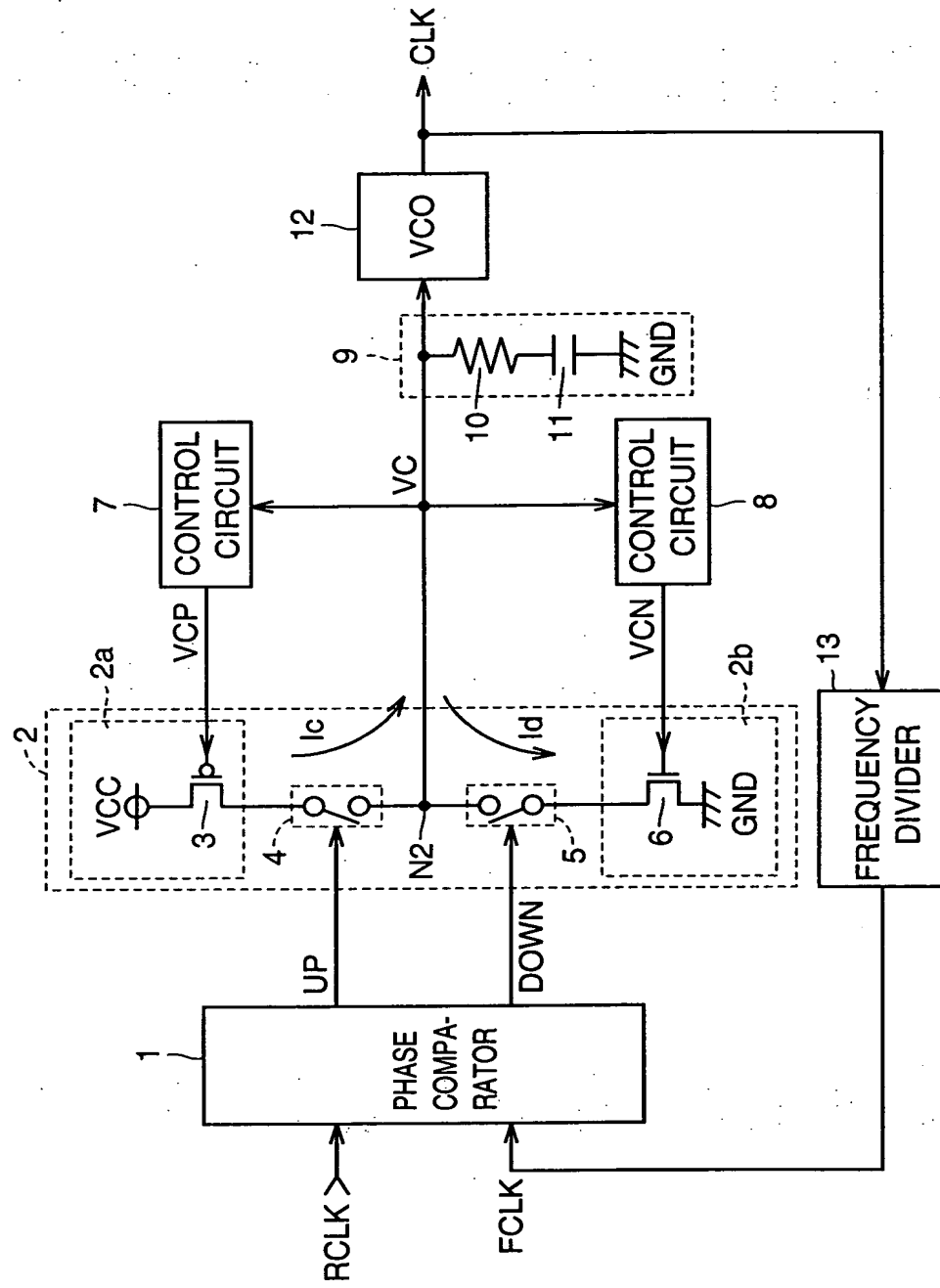


FIG.2

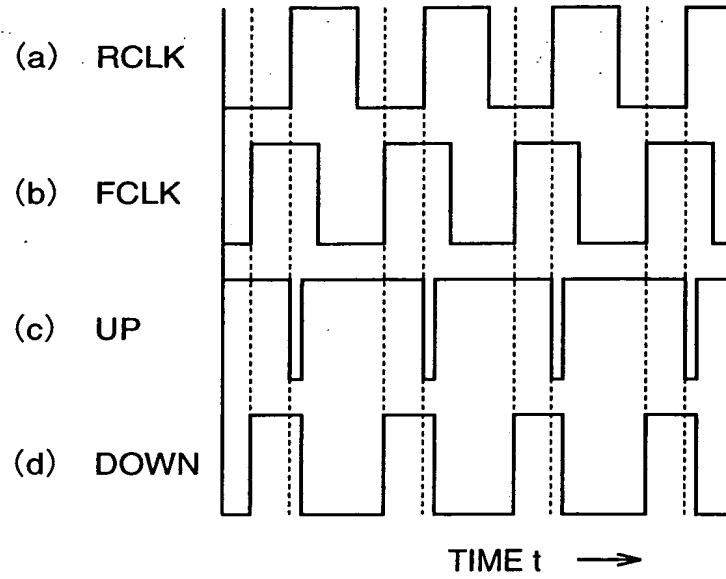


FIG.3

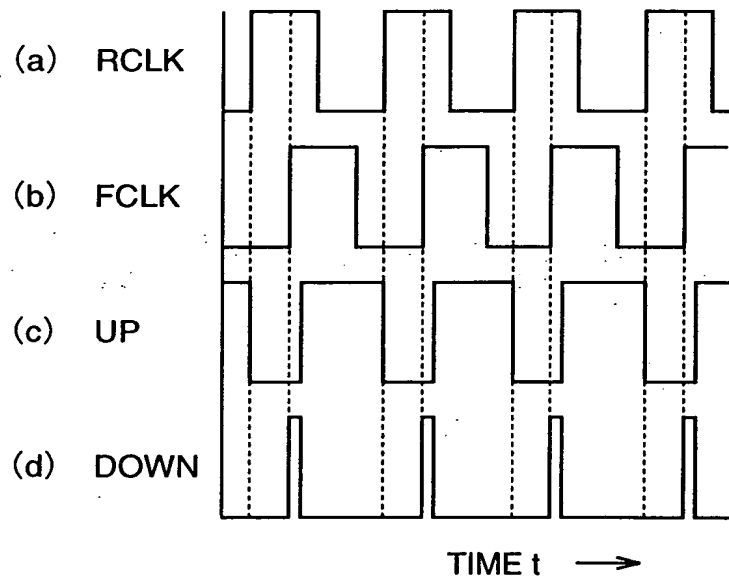


FIG.4

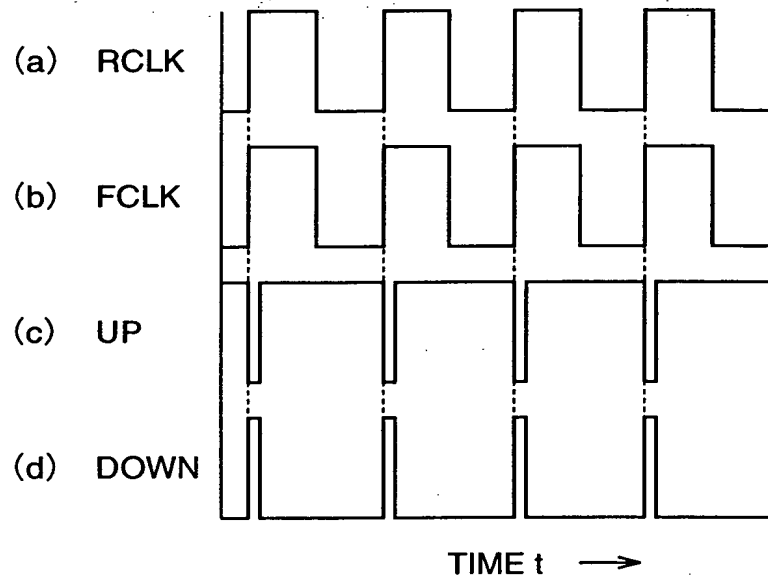
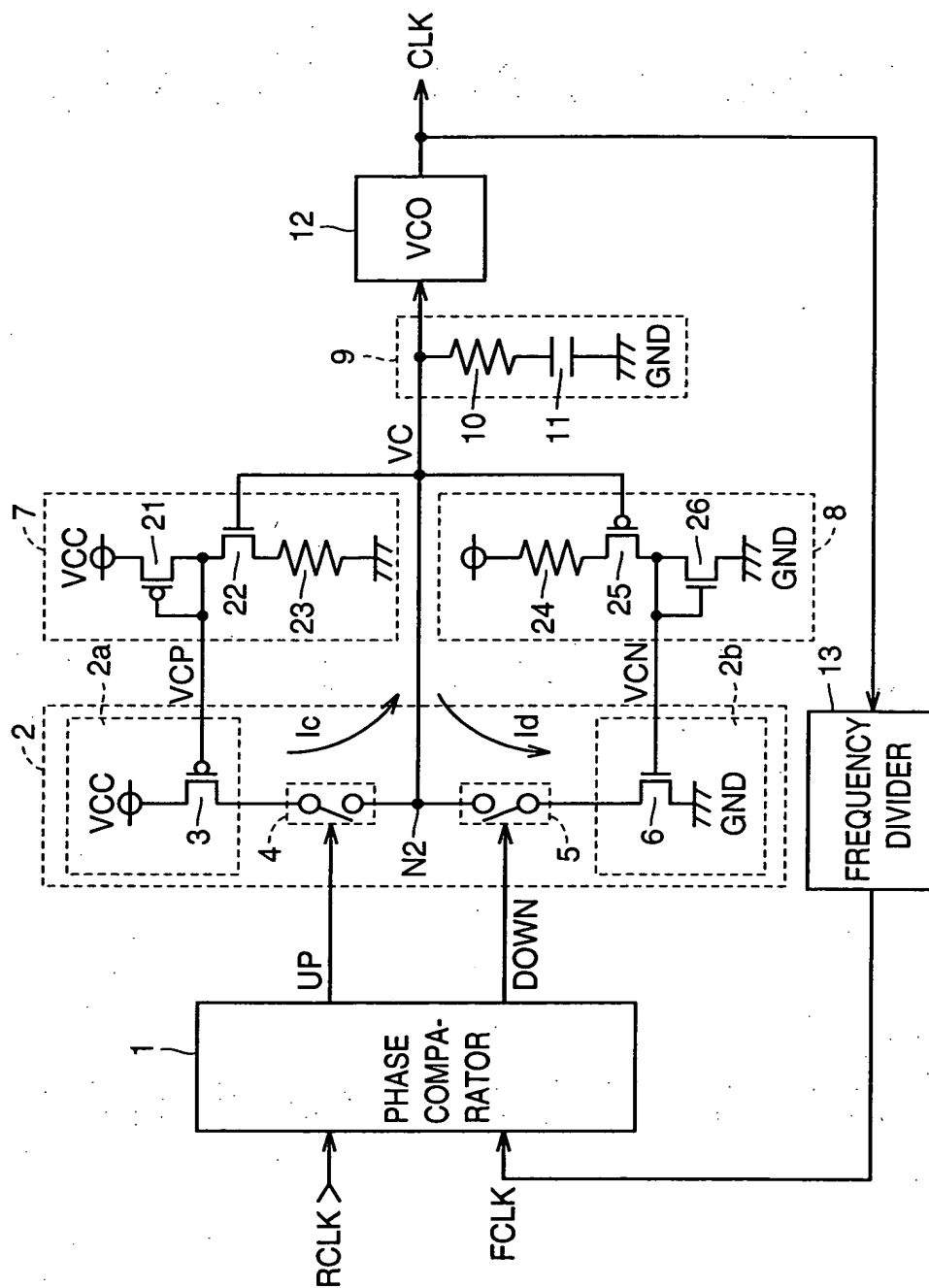


FIG.5



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FIG.6

12

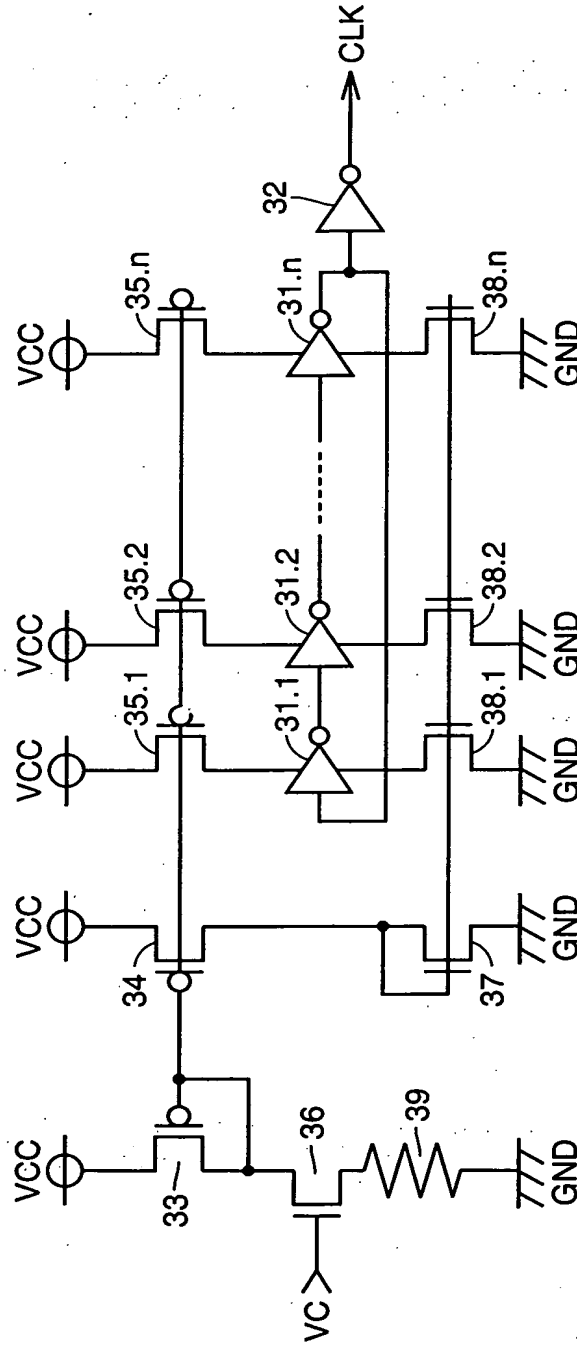


FIG.7

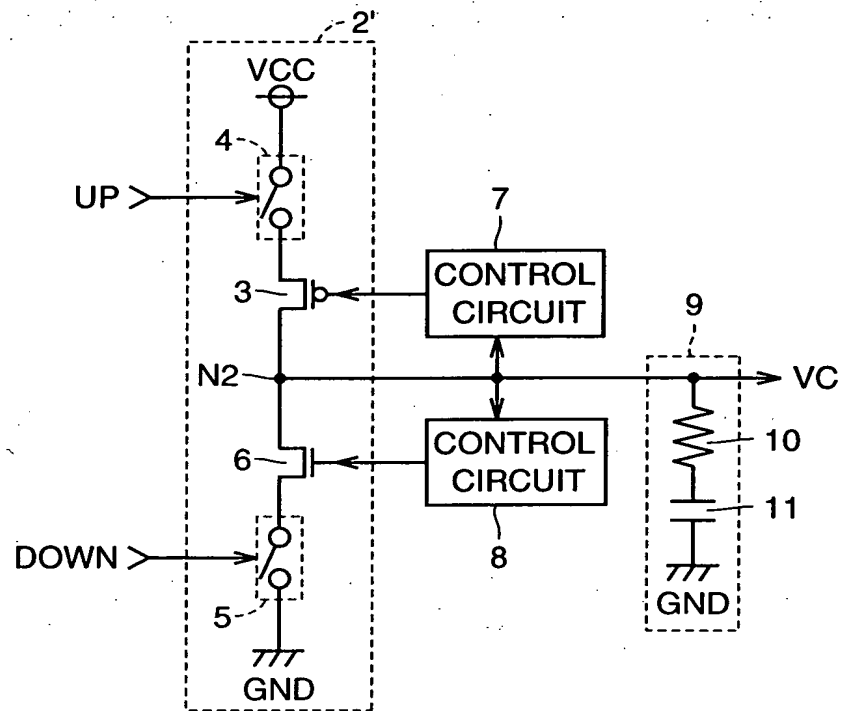
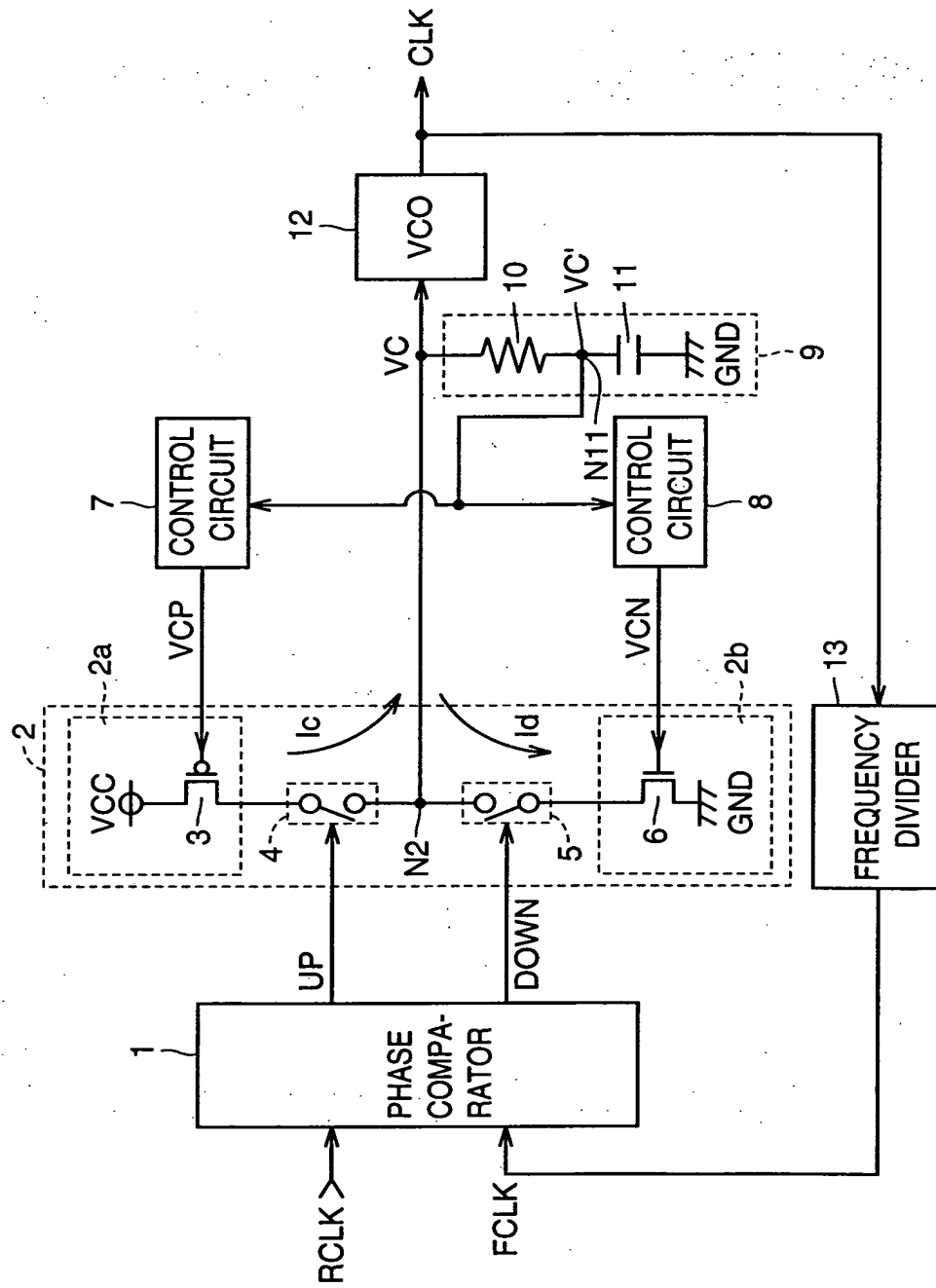


FIG.8



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FIG.9

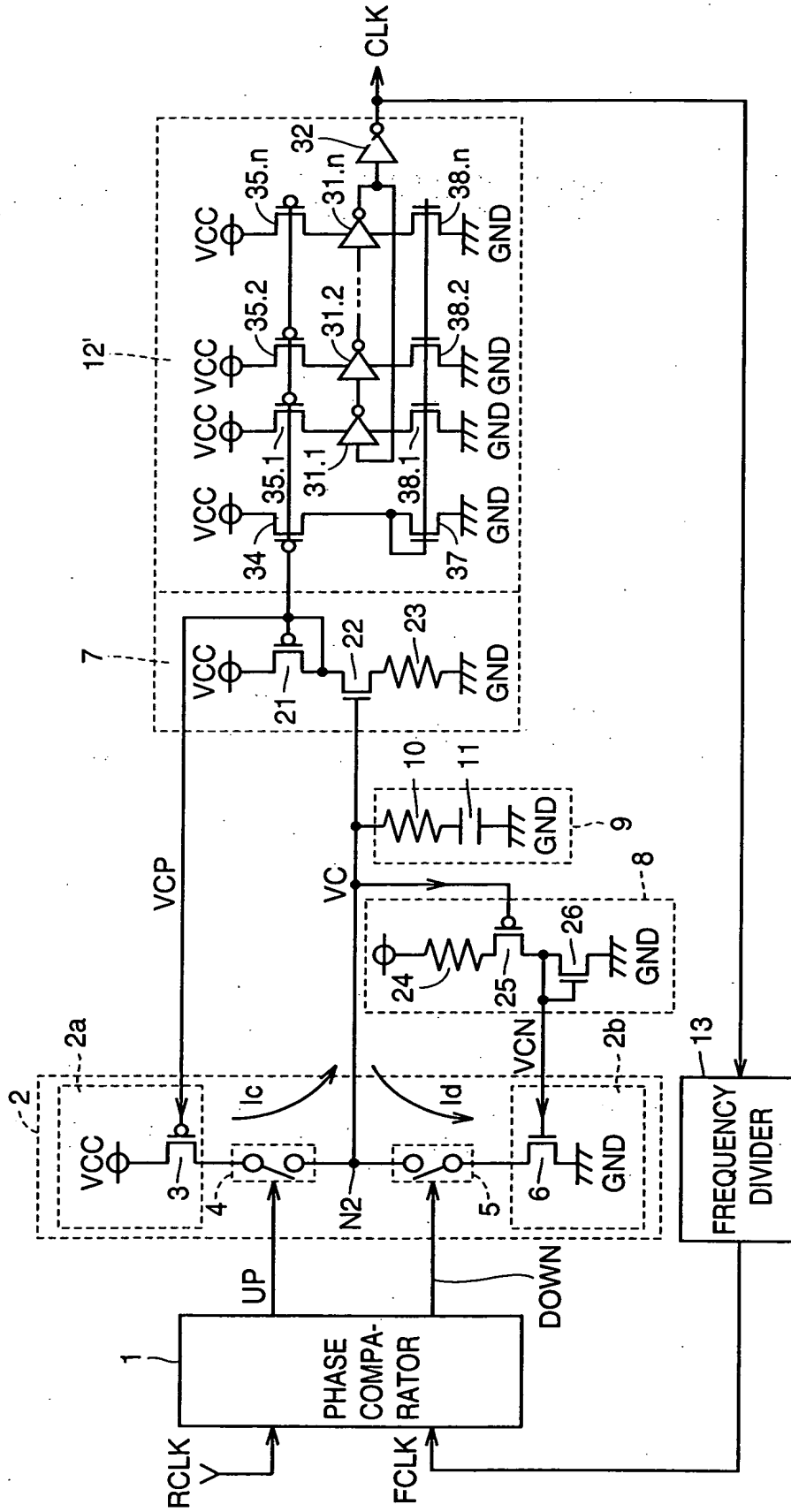
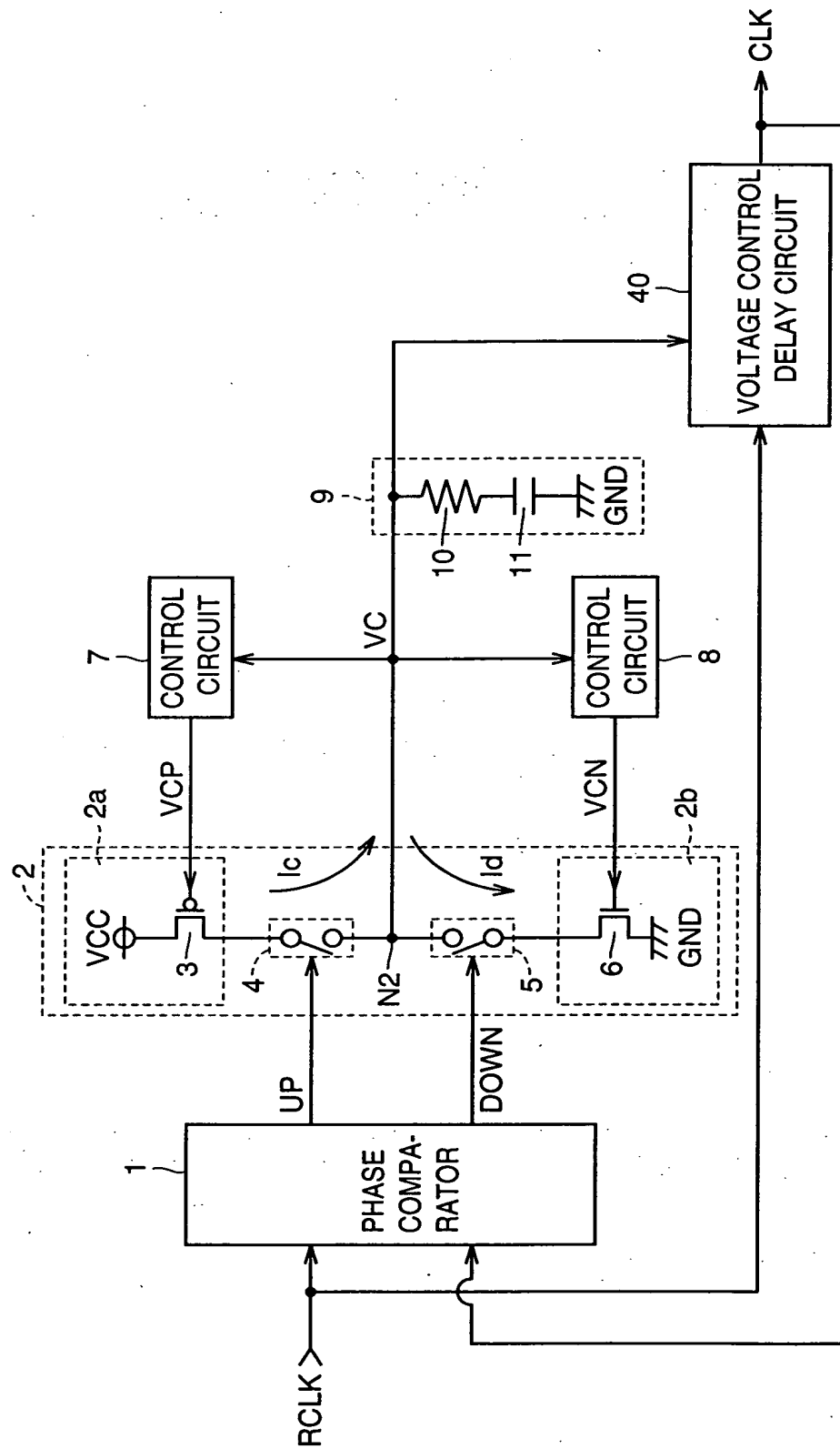




FIG.10



The diagram shows a circuit 41 enclosed in a dashed rectangle. It contains two comparators, 41a and 41b, and two switches, 4 and 5. Comparator 41a is at the top, with its non-inverting input (3) connected to VCC and its inverting input (42) connected to VBP. Its output is VCP. Comparator 41b is at the bottom, with its non-inverting input (6) connected to GND and its inverting input (43) connected to VBN. Its output is also VCP. Between the comparators are two switches, 4 and 5, each controlled by UP and DOWN signals. The output of comparator 41a is connected to switch 4, which is connected to node N2. Node N2 is connected to switch 5, which is connected to the input of comparator 41b. The output of comparator 41b is also VCP.

44

The circuit diagram shows a differential amplifier with a current mirror load. The input differential pair consists of NMOS transistors 45 and 46. The gates of both transistors are connected to a common bias voltage VBP. The source of transistor 45 is connected to the source of transistor 46, which is in turn connected to the gates of PMOS transistors 47 and 48. The gates of PMOS transistors 47 and 48 are connected to a common bias voltage VBN. The drain of transistor 45 is connected to VCC. The drain of transistor 46 is connected to VCC through a resistor 48. The output of the differential pair is taken from the drain of transistor 46. The circuit is powered by VCC and GND.

FIG.13

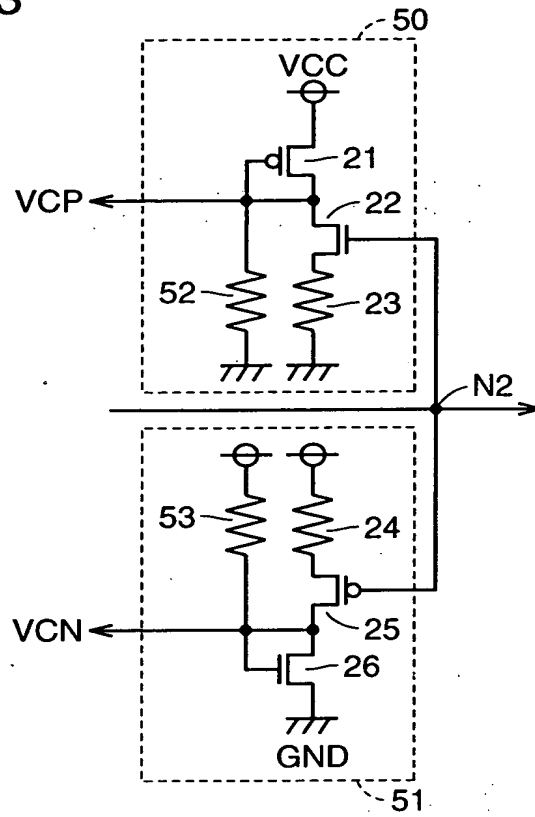


FIG.14

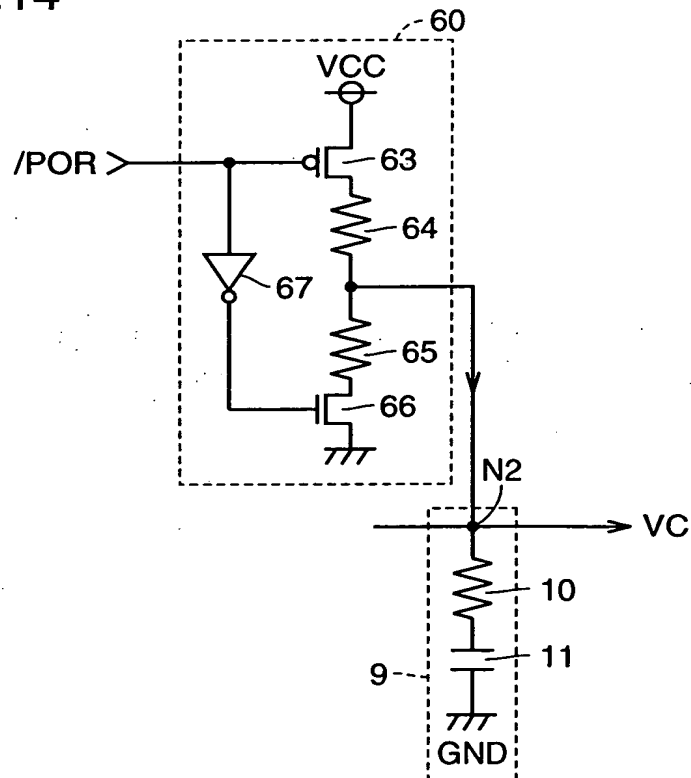


FIG. 15

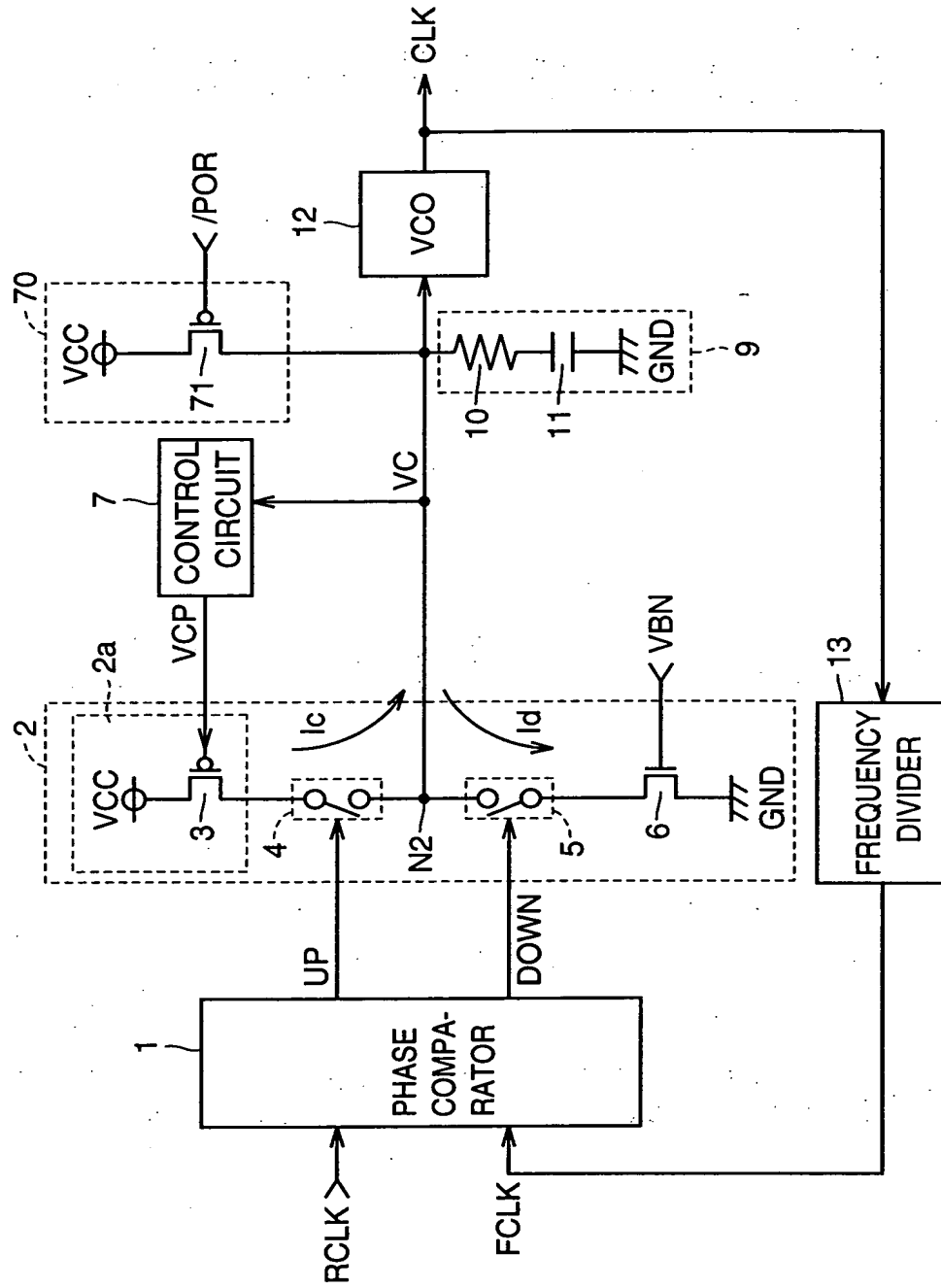


FIG. 16

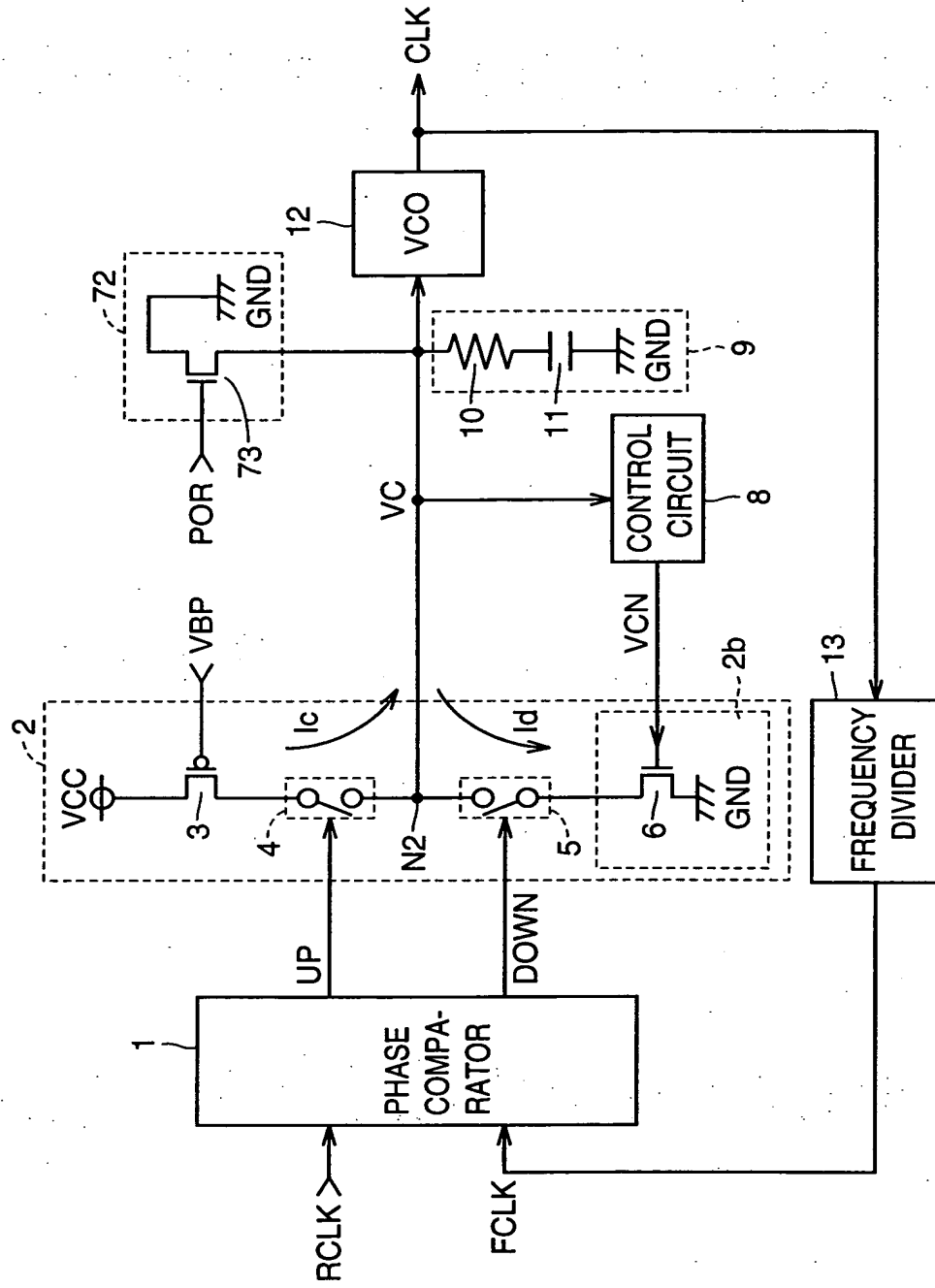
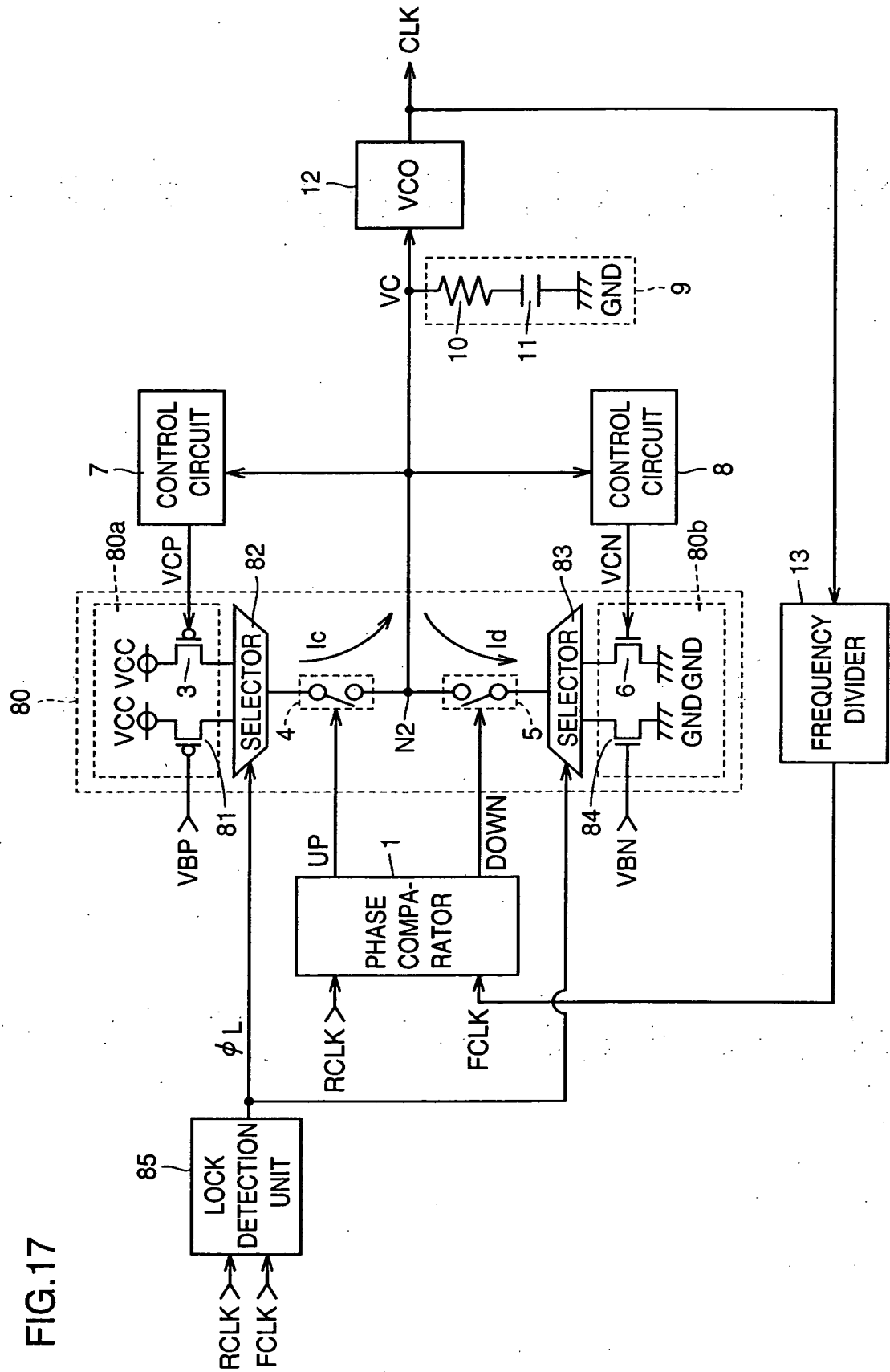


FIG. 17



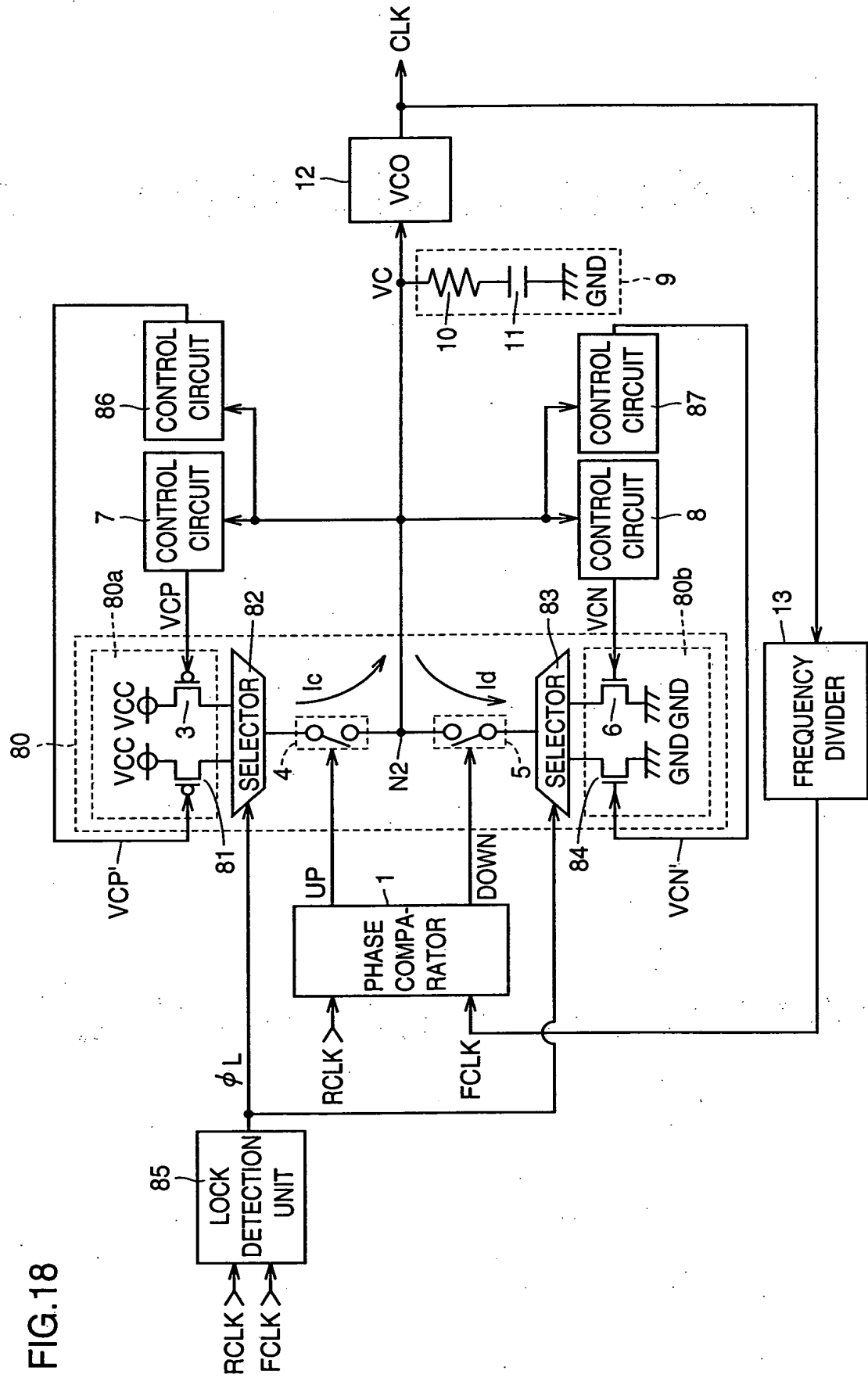


FIG.19

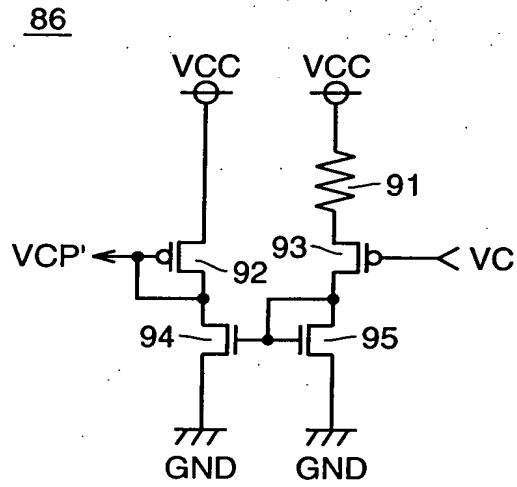


FIG.20

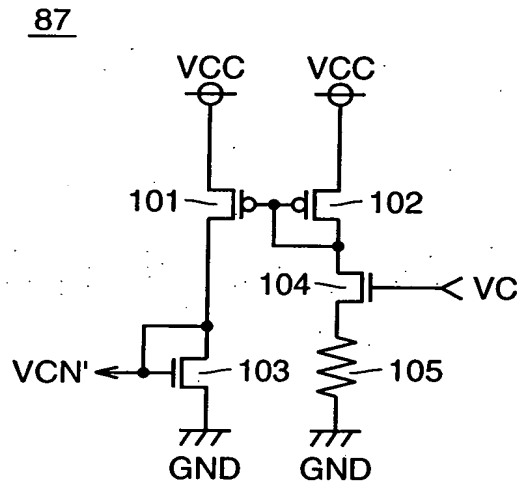






FIG.22

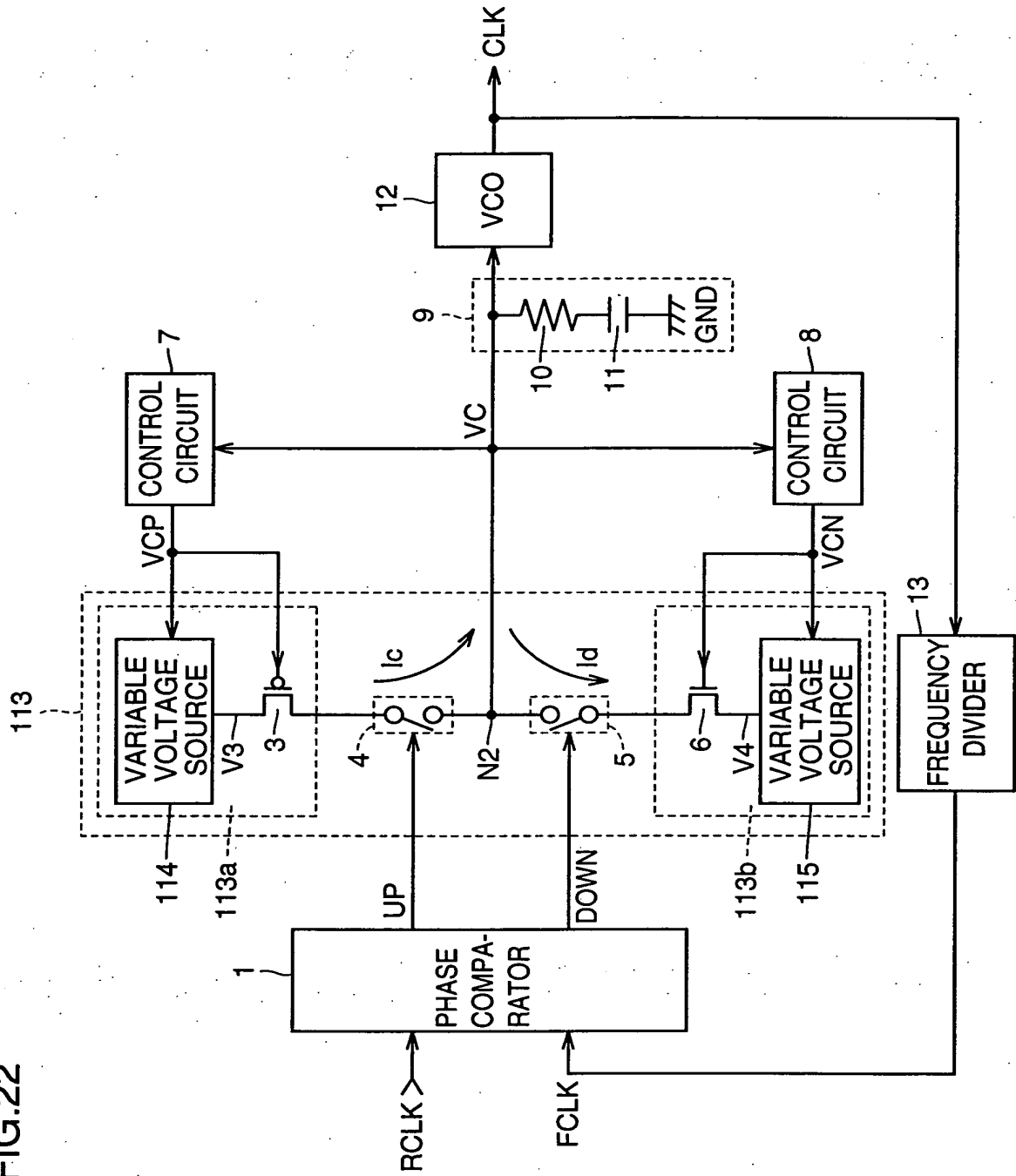


FIG.23 PRIOR ART

